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Isolated EWiRaC: A New Low-Stress Single-Stage Isolated PFC Converter

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Abstract- **A new PFC-family of Efficient Wide Range Converters named EWiRaC was recently introduced. EWiRaC has a major advantage in terms of efficiency at low-line and handles challenges like inrush current limiting as an integrated part of the conversion scheme. The main objective of this paper is to investigate the performance of an isolated EWiRaC (I-EWiRaC) in a single-stage PFC configuration.**

I. INTRODUCTION

In a typical dual-stage PFC system a boost converter is used as a power factor correction preregulator. A cascading dc-dc converter provides isolation and an output voltage lower than the peak input voltage. The boost topology is in particular a good choice for ac/dc conversion but at low line the larger step-up ratio results in great losses in the boost switch.

The EWiRaC places the boost converter in a more ideal setup by inserting a voltage source between the input and the output. This modifies the volt-seconds applied to the boost inductor and enables the output voltage of the PFC stage to be lower than the input voltage. This approach is called the "series voltage source approach" [1,2,3,4]. By isolating the EWiRaC the whole PFC scheme is made possible in a single stage. The I-EWiRaC evolution is shown in Fig. 1.

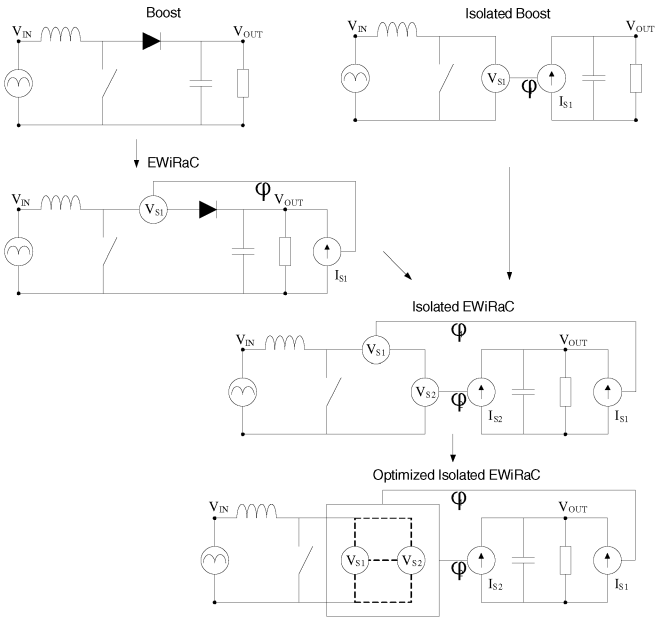

Fig. 1. The I-EWiRaC evolution.

II. THE BASIC IDEA BEHIND I-EWIRAC

Isolation is integrated with a voltage source as done in the isolated boost shown in Fig. 1. The power obtained by the two voltage-sources is transferred and delivered to the current-sources in parallel with the output. In order to reduce the voltage source stress an optimized solution for the I-EWiRaC is preferred making it possible to couple the voltage sources in parallel. The voltage sources can be coupled as shown in Fig. 2. The reflected output voltage Vs = Vs1 = Vs2.

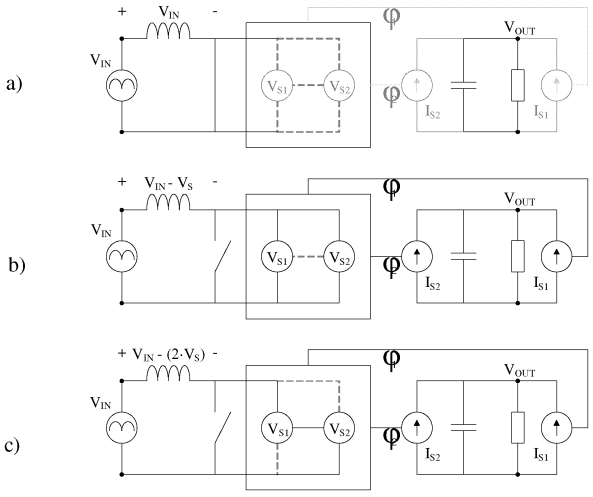

Fig. 2. Couplings. a) Short-circuit b) Parallel c) Series

I-EWiRaC changes operating mode according to the line voltage by switching between two configurations of the boost topology. If the input voltage is below the reflected output voltage the voltage-sources are either short-circuited for charging the inductor or in parallel for discharging. This can be recognized as a standard isolated boost mode.

If the input voltage rises above the reflected output voltage a mode-shift occurs. The voltage-sources are now coupled in parallel for charging the inductor or in series for discharging. In this mode the converter operates in step-down mode but still like a boost.

Inrush current limiting is naturally incorporated in the EWiRaC [2] and into I-EWiRaC because they has the ability to control the output voltage even though the input voltage is higher than the output voltage. This comes in handy when starting up the converter or subsequent units are defective.

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III. A PRACTICAL IMPLEMENTATION

An implementation of the I-EWiRaC is shown in Fig. 3. The voltage-sources are replaced by full-bridge configured transformers [1,3]. The transformers turn ratio used in this paper was 1:1. The input to the converter is the rectified input voltage shown in Fig. 4.

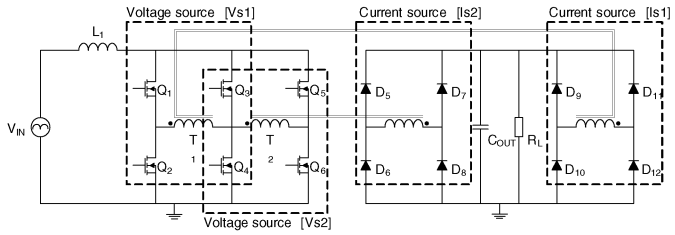

Fig. 3. Full-bridge configuration of an I-EWiRaC

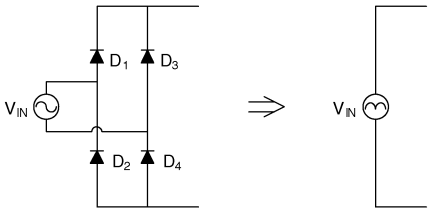

Fig. 4. Rectified input voltage

A. *Step-up mode: Vin<reflected Vout*

I-EWiRaC has a major advantage considering component stress level. By sharing the inductor current low stress levels of the transistors, transformers and diodes are obtained in both operating modes. CCM operation was chosen because it offers several benefits like a low inductor current ripple and a smaller EMI filter.

When all transistors are activated the inductor is charged and the load is supplied entirely by the output storage capacitor. A parallel coupling discharges the inductor and is made by activating Q_1, Q_4, and Q_6 or Q_2, Q_3 and Q_5. By alternating the two parallel couplings in every switching period the current in the transformer windings are constantly interchanged. This is done to prevent saturation and insure optimal use of the transformer BH-loop. The interchange is used for the parallel and series couplings in both modes. The converter switching frequency used in this research was set to fs=1/T=70kHz which corresponds to T=14uS. The switching frequency of the transformers became 35kHz because of the interchanging.

The step-up mode conversion ratio is given by

$$\frac{Vout}{Vin} = \frac{n}{1-d_1} \qquad (1)$$

where n is the transformers turn ratio and d_1 is the duty cycle for this mode.

The switching pattern for this mode is shown in Fig. 5 and a timing diagram for the voltages and currents of interest are shown in Fig. 6.

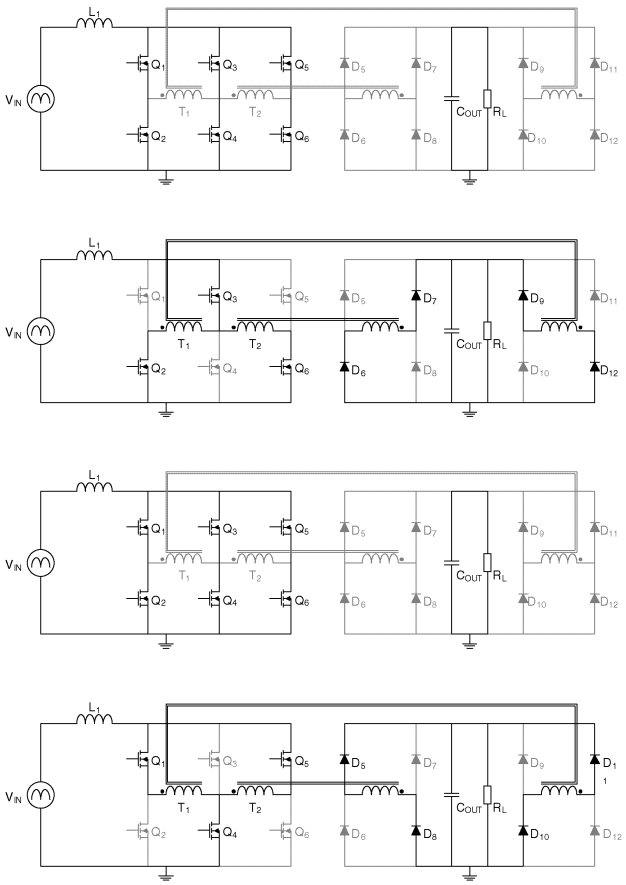

Fig. 5. Short-circuit and parallel couplings

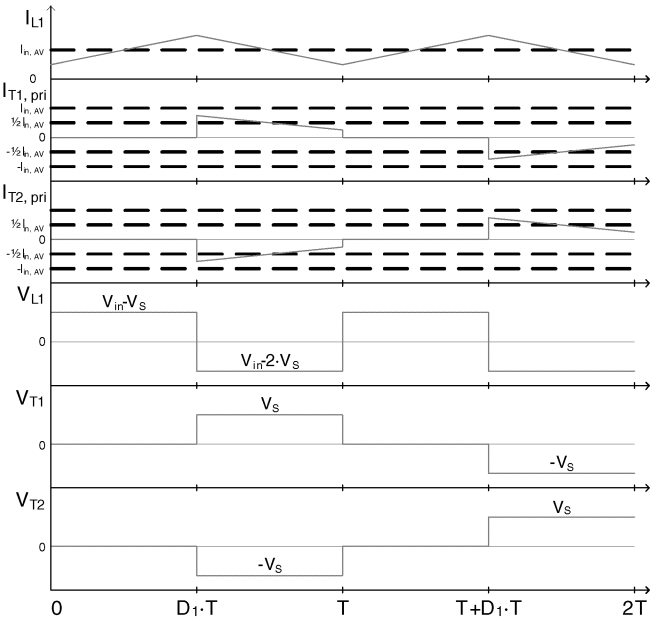

Fig. 6. Timing diagram for circuit currents and voltages in step-up mode

B. Step-down mode: Vin>reflected Vout

In this mode a parallel coupling is charging the inductor due to the changed relationship between the input and output voltage. The shifting pattern for this mode is shown in Fig. 7.

A series coupling is made by activating Q1 and Q6 or Q2 and Q5. This will discharge the inductor because the reflected voltage from the transformers on the right side of the inductor is 2 times the output reflected voltage which is larger than the input voltage.

In step down mode the conversion ratio is given by

$$\frac{Vout}{Vin} = \frac{n}{2 - d_2} \tag{2}$$

where n is the transformers turn ratio and d_2 is the duty cycle for this mode.

A timing diagram for the voltages and currents of interest is shown in Fig. 8.

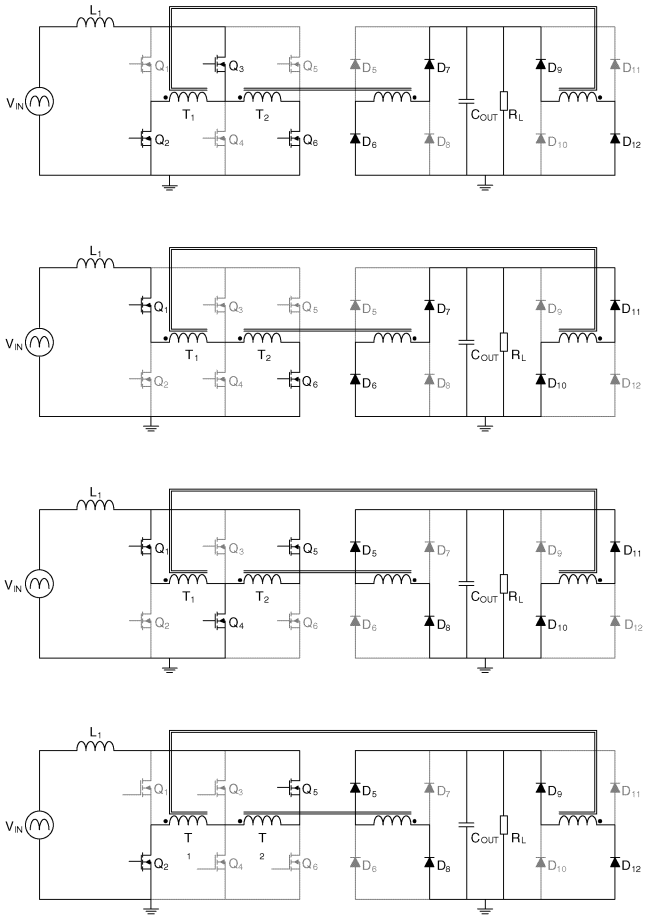

Fig. 7. Parallel and series couplings

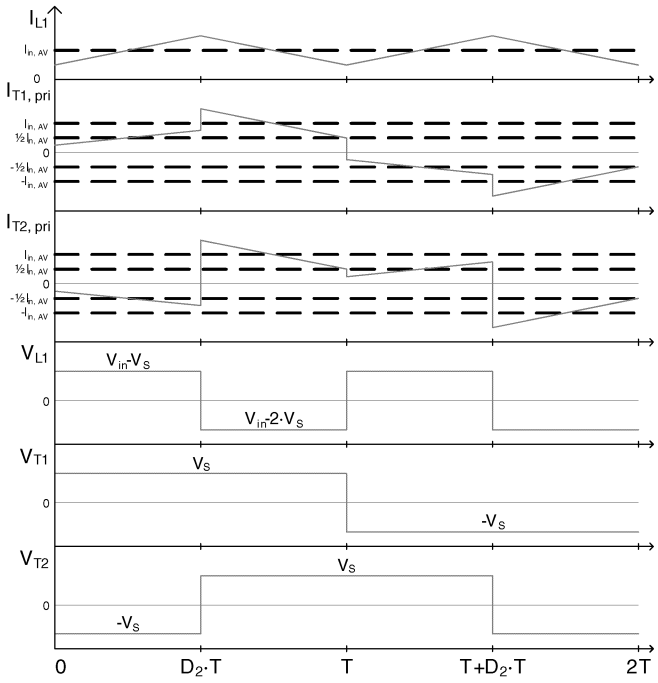

Fig. 8. Timing diagram for circuit currents and voltages in step-down mode

C. Operating range

Fig. 9 shows the conversion ratio in the two modes. I-EWiRaC has no restrictions regarding the output voltage due to the transformer turn ratio. The duty-cycles changes drastically around the mode-shift and with a turn ratio of 1:1 the I-EWiRaC has a minimum output limit given by

$$\frac{270V \cdot \sqrt{2}}{2} < V_{OUT} \tag{3}$$

The limit is set by the step-down conversion ratio M(d2) shown in Fig. 9. The EWiRaC can also be used in DC-DC conversion where the DC input voltage range varies significantly

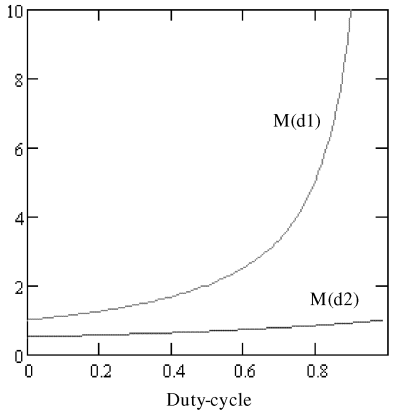

Fig. 9. Step up mode and step down mode conversion ratios

IV. ISOLATED EWIRAC VS. ISOLATED BOOST

I-EWiRaC substitute the isolated boost converter used in many single staged PFC schemes. It is therefore natural to compare the I-EWiRaC with an isolated boost like the one shown in Fig. 10.

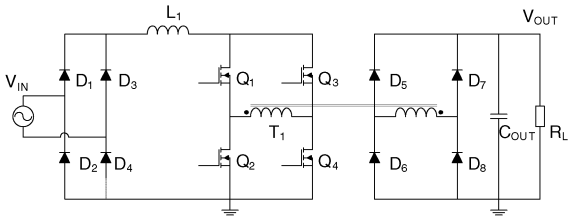

Fig. 10. Full-bridge isolated boost (prior art)

Table I shows component conditions for an isolated boost delivering 400V@500W and an I-EWiRaC delivering 200V@500W. In this case the transformer turn ratio was 1:1.

TABLE I
ELECTRIC V ALUES FOR POWER COMPONENT S

Comp.	**Isolated Boost**			**Isolated EWiRaC**		
	Vpeak	*Irms*^{2}	*Iavg*	*Vpeak*	*Irms*^{2}	*Iavg*
Q(1,2,5,6)	400	15.5	-	200	8.94	-
Q(3,4)	-	-	-	200	13.11	-
D1-D4	400	4.17	0.63	200	2.1	0.63
D5-D8	-	-	-	200	2.1	0.63
	Vdc	*Irms*	*(Vdc· Irms)*^{2}	*Vdc*	*Irms*	*(Vdc· Irms)*^{2}
C	400	2.6	1.08M	200	2.6	0.27M
	Av. V_L	*Vol.* cm^3	-	*Av.* V_L	*Vol.* cm^3	-
L	81	32	-	40.5	16	-
Transfor-mer 1	-	100	-	-	28	-
Transfor-mer 2	-	-	-	-	28	-

The two extra transistors in the I-EWiRaC are not necessarily increasing the actual cost and size of the converter. The necessary amount of silicium for the transistors is basically determined by the transistors peak voltage and conduction currents. The summed values of these variables are almost the same for the two converters and thus the cost and size is unchanged.

The four extra diodes in the I-EWiRaC are increasing the diode count by a factor of two as well as the electrical condition of the diodes are decreased by a factor of 2. Again the component count suffers most in this comparison.

The voltage demand and volume of the output capacitor is decreased with the I-EWiRaC due to the decrease in Irms-, Vcap-product.

The volume of the inductor and transformers is actually smaller in the I-EWiRaC. This is caused by a reduction in the applied volt-second product.

The comparison shows that component -volume, -weight and -price in the power stage won't change much. I-EWiRaC has a lower component stress level that will decrease the need for cooling. Marketing wise the higher efficiency can be exploited in terms of a "Green Technology"-scheme.

V. EXPERIMENTAL WORK

A 500W version of the I-EWiRaC with 185V on the output and a switching frequency of 70kHz has been build and tested for universal voltage mains range operation. Fig. 11. shows the prototype.

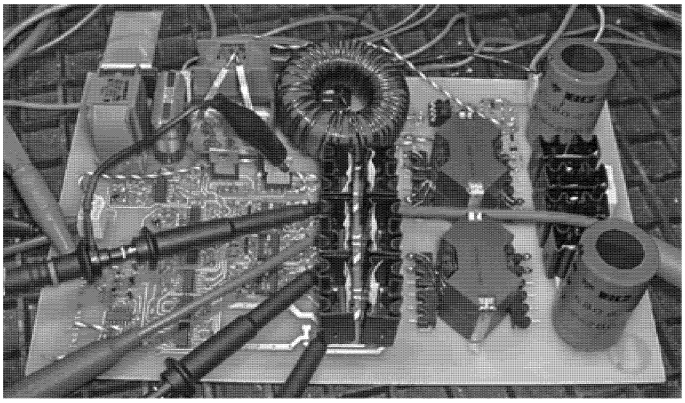

Fig. 11. Prototype of the I-EWiRaC

D. Control

The most interesting task was to design a control system that could handle the mode shift well and provide the right duty cycle and switch patterns for six switches. The control scheme is shown in Fig. 12.

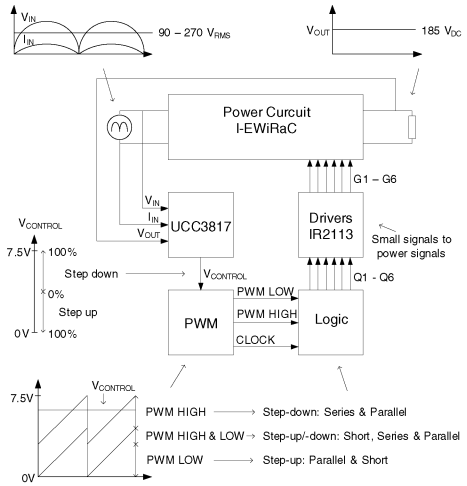

Fig. 12. Control diagram

The UCC3817 is a PFC controller that uses average current mode control in order to maintain a stable, low distortion sinusoidal line current [5]. It produces a control signal that commands an internal PWM to force the correct current. The internal PWM is not designed for switching duty-cycles so the control signal is feed to an external dual PWM circuit.

The PWM signals needed is made by comparing the control signal with 2 saw toothed curves where one of the curves is level shifted as seen in Fig. 13. The drawback of this approach is that an overlap of the saw tooth curves is unavoidable and it introduces an extra unwanted mode shift.

The logic circuit receives the two PWM signals and a signal called CLOCK. CLOCK enables the logic to determine when to switch between the two different parallel and series couplings of the transformers. The PWM, gate and logic signals for the step up and step down modes plus the extra mode are shown in Fig. 13.

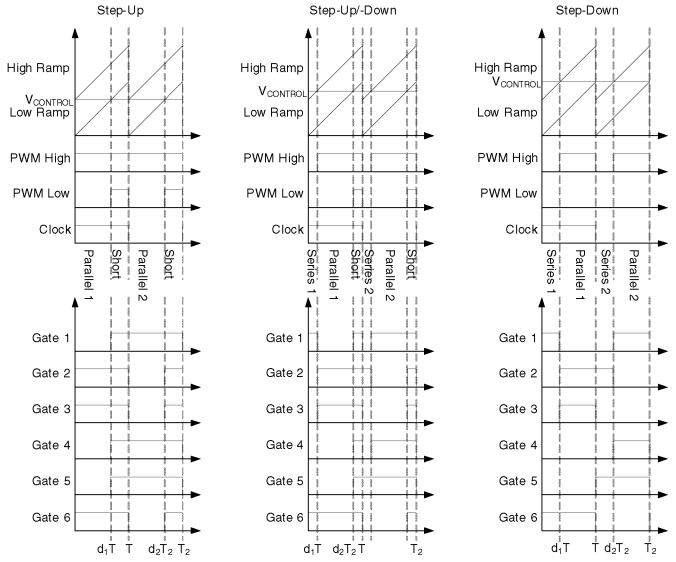

Fig. 13. PWM, logic, and gate signals

The PWM circuit is mainly made out of three LM431 comperators. One is making the actual sawtooth ramp while the two others are comparing the control signal from the UCC3817 with the original and level shifted sawtooth ramp. The logic block is build with simple AC74XX logic gates.

E. Step up/down mode

As mentioned an extra mode shift is introduced when creating the PWM signals. In this mode the voltage sources are coupled in series, in parallel and then short-circuited.

The conversion ratio for this mode is given by

$$\frac{Vout}{Vin} = \frac{-n}{d1 + d2 - 2} \qquad (2)$$

A step-up conversion occurs when the input voltage is under the output voltage and a step-down conversion occurs for the opposite. The mode-shift voltages and duty-cycle variation is a function of the input voltage which is shown in Fig. 14.

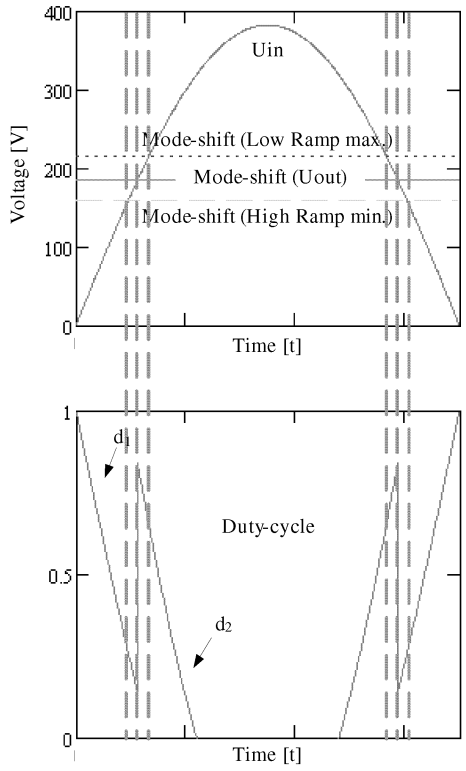

Fig. 14. Input voltage, mode-shift voltages and duty-cycle.

F. Calculated losses and effeciency

The worst case operation for the I-EWiRaC occurs in step up mode at low line. The choice of power components is based on calculations for that mode to insure the highest possible efficiency. Table 1 shows the estimated losses for the chosen power components.

TABLE II
CALCULATED WORST CASE LOSSES FOR I-EWIRAC (V_{IN}=90V)

Component	Type	Losses	% of P_{IN}
EMI-filter	2·2.7mH, 8A, Rdc=22mΩ	1.5W	0.3%
Bridge Rectifier	GBU8J, 8A, 600V	9.3W	1.7%
Inductor	A083081, Ve=11cm^3, N=49, d_{cu}=1.06mm	3.2W	0.6%
Mosfets	6·STP20NM50, Ron=80mΩ	13.2W	2.4%
Transformers	2·RM12, Np=42, d_{cu}=0.8mm	4.4W	0.8%
Diodes	8·STTH806TTI	8.4W	1.6%
Total		40W	7.4%

The numbers in table 1 is only used as a guideline for choosing the right components. A total loss of 40W gives an efficiency around 92% which is 2.5% higher than measured.

G. Results

Fig. 15 shows a measurement of the input current harmonics. The Power factor is near unity due to the low distortion average current controlled PFC and the I-EwiRaC complies with EN61000-3-2.

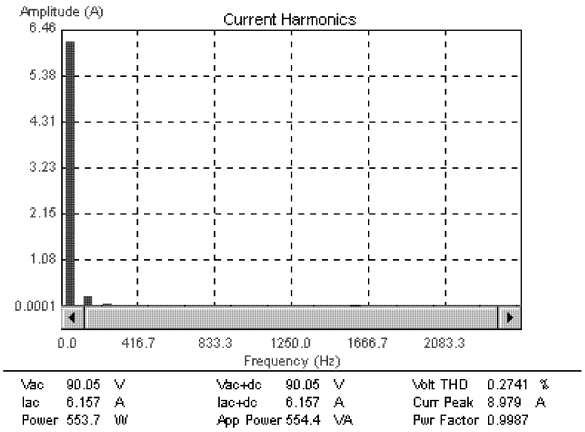

Fig. 15. Input current harmonics at Vin =90Vac and Pout=500W

Fig. 16 shows a measurement of the input current vs. the input voltage at full power.

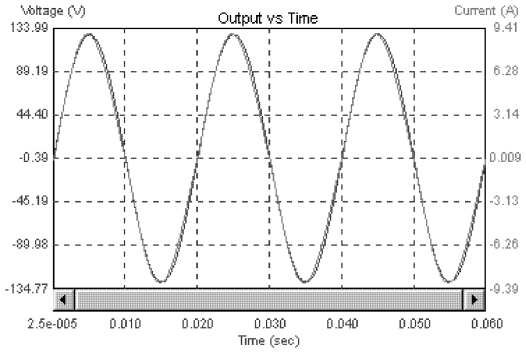

Fig. 16. Input current vs. input voltage at Vin=90Vac and Pout=500W

I-EWiRaC also has a well shaped current at lower power as shown in Fig. 17

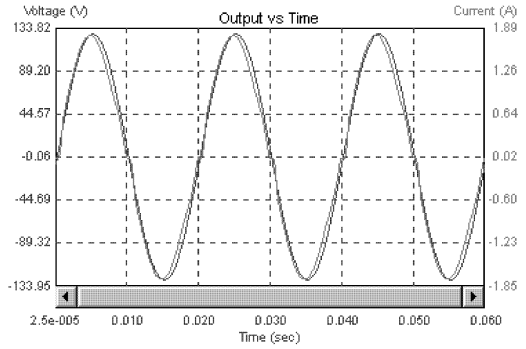

Fig. 17. Input current vs. input voltage at Vin=90Vac and Pout=100W

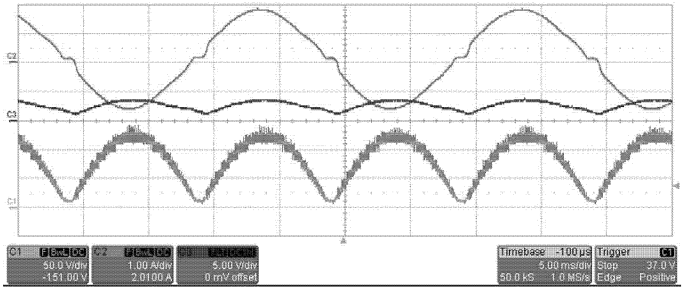

Fig. 18. Input current (top), control signal (middle) and average transistor voltage (bottom).

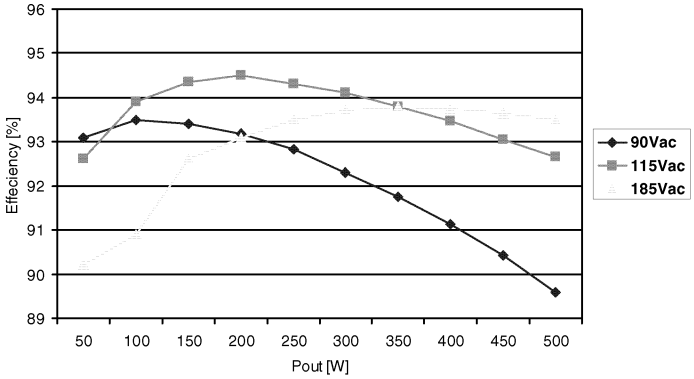

Fig. 19. Effeciency

VI. Conclusion

An isolated EWiRaC PFC converter and principle of operation has been introduced. A 500W model has been build and tested experimentally. The converter exhibits these advantages: Universal mains input voltage range, inrush current limit, galvanic isolation, improved low-line efficiency, and reduced component stress as compared to a dual stage PFC system. Thus the isolated single-stage PFC converter is "reborn".

Acknowledgement

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